

# See One, Do One, Teach One

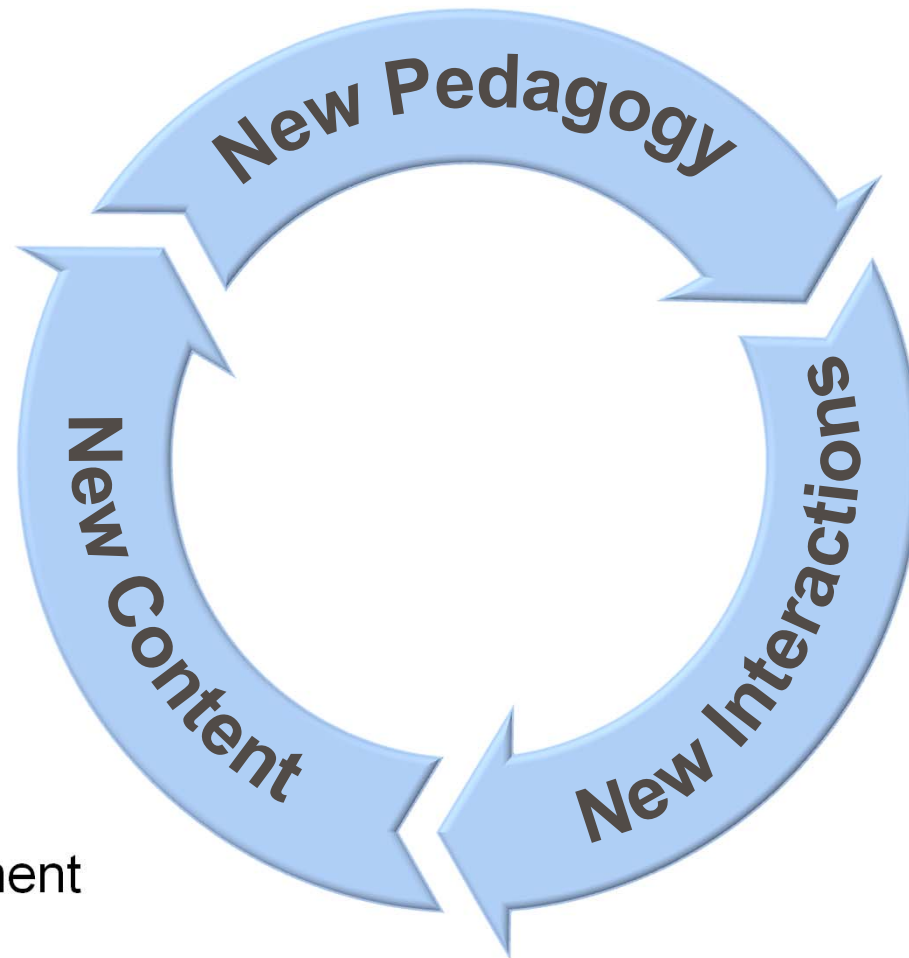
**Chris Terman**

Senior Lecturer, MIT Dept. of EECS

*This work is supported by T-Party & Project Qmulus, a 10-year research collaboration between Quanta Computer, Inc., and CSAIL*

# Research in Educational Technology @ CSAIL

- Self-paced mastery learning
- Hands-on learning
- MOOC as education laboratories
- Measure results → target improvements



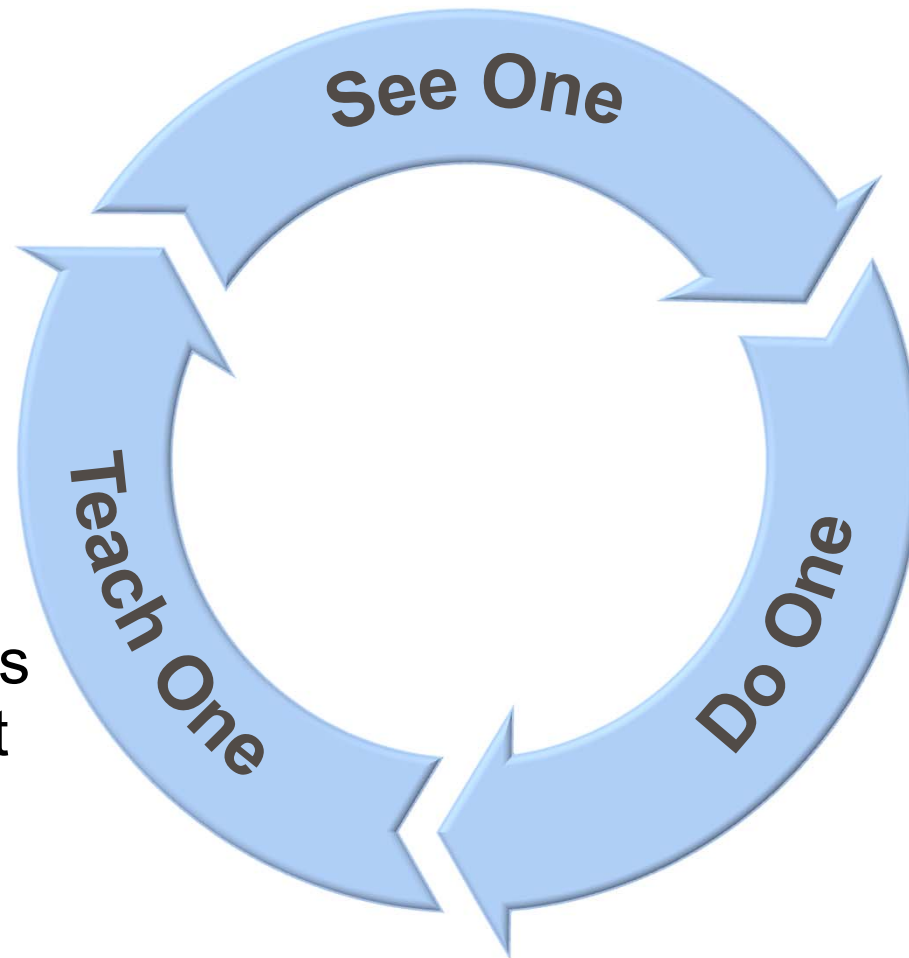
- Curricular API
- Authoring tools
  - Visualizations
  - Interactions
- Automate assessment

- Forum summaries
- Search/navigation
- Learning networks
- Learner sourcing



# Achieving mastery

- Novice**
- Learn concepts
  - Observe skills
  - Analyze
  - Understand *what*



- Master**
- Teach concepts
  - Demonstrate skills
  - Organize/connect
  - Explain *why*

- Apprentice**
- Apply concepts
  - Practice skills
  - Synthesize
  - Learn *how*



# See One: Effective learning sequences

Recipe: Short video → interaction → repeat

The screenshot shows a courseware interface with a navigation menu on the left and a video player in the center. The navigation menu includes links for Courseware, Course Info, Textbook, Discussion, Wiki, Progress, and Instructor. The video player is titled "S8V5: ANOTHER DEPENDENT SOURCE EXAMPLE" and shows a circuit diagram with a dependent current source labeled "VCCS". The video player has a progress bar at 0:23 / 3:34, a speed control set to 1.50x, and various playback controls. The video content includes a circuit diagram and a transcript of the instructor's explanation.

Courseware Course Info Textbook Discussion Wiki Progress Instructor

Overview  
Week 1  
Week 2  
Week 3  
Week 4  
Incremental Analysis  
Lecture Sequence  
Dependent Sources and Amplifiers  
Lecture Sequence  
Week 4 Tutorials  
Homework 4  
Homework due Oct 07, 2012 at 00:00 UTC  
Lab 4  
Lab due Oct 07, 2012 at 00:00 UTC  
Week 5  
Week 6

S8V5: ANOTHER DEPENDENT SOURCE EXAMPLE

Another dependent source example

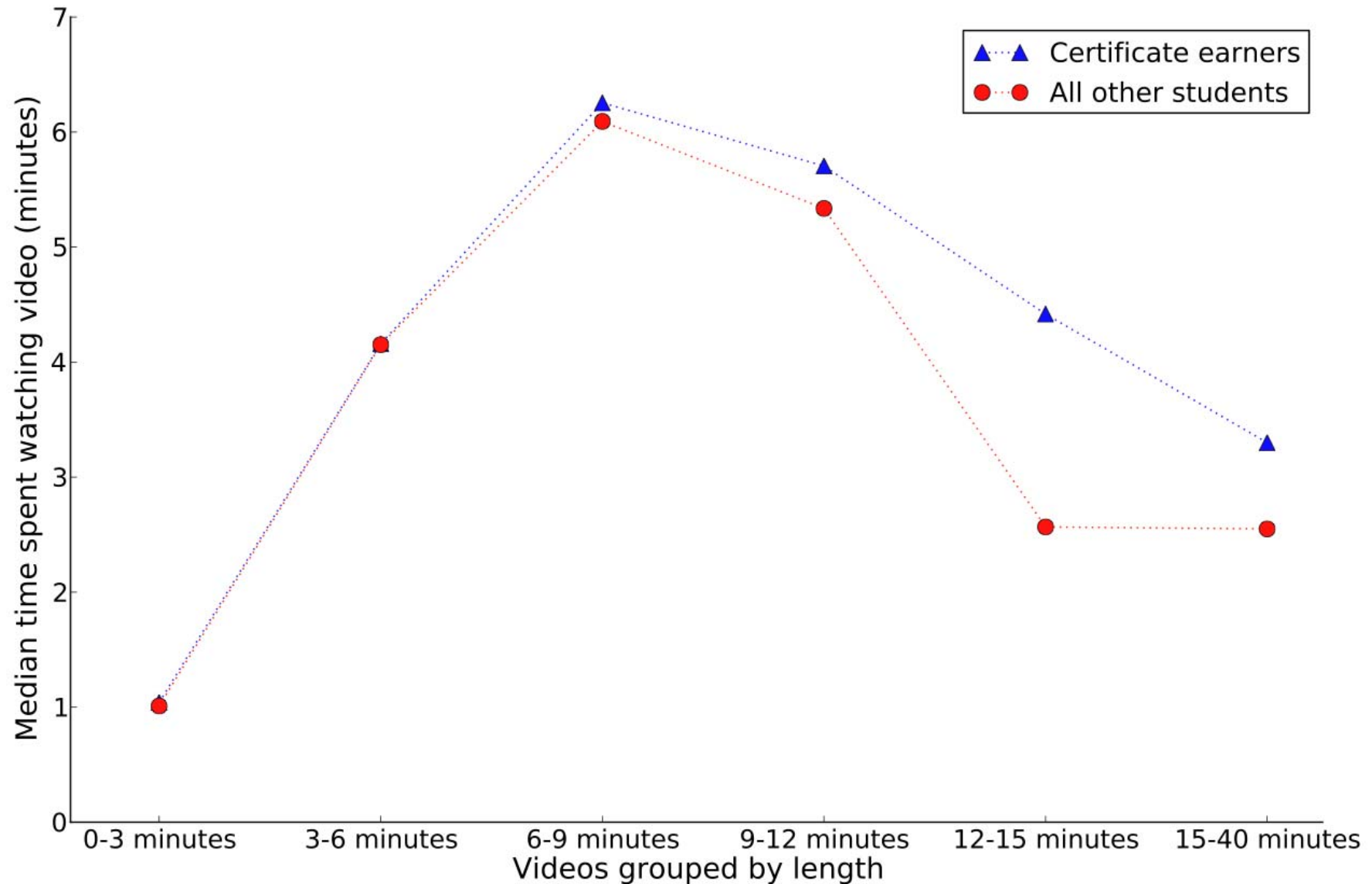
And you have the output port here. So what I'm going to do is in this particular circuit, I'm going to connect a voltage source at the input, an independent voltage source at the input,  $V_i$ . And I'm going to connect the output as follows. I'm going to connect a resistor to the output as follows. I'm going to call it  $R_L$  for load resistor. This terminal is going to be connected to ground. And then I'm going to connect the  $R_L$

Download video [here](#).

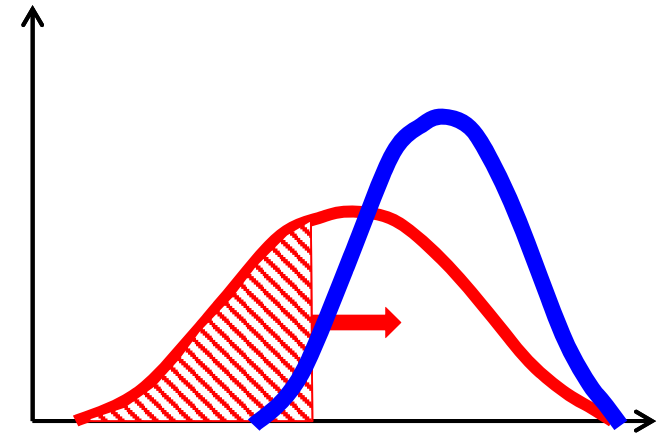
Challenge: it's not a captive audience!



# See One: Attention span data



# See One: Mastery learning

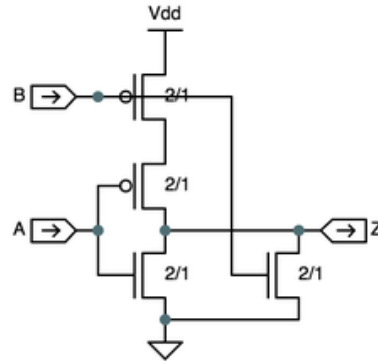


Help

- › 1. Basics of Information
- › 2. The Digital Abstraction
- › Assignment 1 (due Apr 14)
- 3. CMOS
  - Lecture Videos (44:58)
  - Worked Examples
  - Tutorial Problems
- › 4. Combinational Logic
- › Assignment 2 (due Apr 21)
- › 5. Sequential Logic
- › 6. Finite State Machines
- › Assignment 3 (due Apr 28)
- › 7. Performance
- › 8. Design Tradeoffs
- › Assignment 4 (due May 5)
- › Exit Survey
- › Exam

## LE3.3.1: CMOS TRUTH TABLE (3/4 points)

Here's another simple CMOS circuit with series PFETs for the pull updown circuit.



Please fill in the truth table below, giving the value of the output Z for the four possible combinations of the inputs values A and B.

A	B	Z	
0	0	<input type="text" value="1"/>	✓ Answer: 1
0	1	<input type="text" value="0"/>	✓ Answer: 0
1	0	<input type="text" value="0"/>	✓ Answer: 0
1	1	<input type="text" value="1"/>	✗ Answer: 0

**Adaptive hints**

### EXPLANATION

When either A or B is 1, the PFETs they control would be OFF and the NFETs they control would be ON. If at least one of the inputs is 1, the series PFET pullup is not conducting, but the parallel NFET pulldown is.

Challenges: useful deadlines & cohorts



# See One: Immediate feedback

Go to go? Or more work to be done?

*I absolutely love the new way of doing problem sets. It lets me know that I am on the right track and helps me understand the problems better.*

*Also, I like how MITx gives quick responses and explanations on what the correct answer is. I wish I had MITx homework problems for all my classes.*

Challenge: avoiding “guess and check”



# Do One: Hands On → Brain On!

“ Learning and retention is related to the depth of mental processing.  
- *Craik and Lockhart*  
1972

”





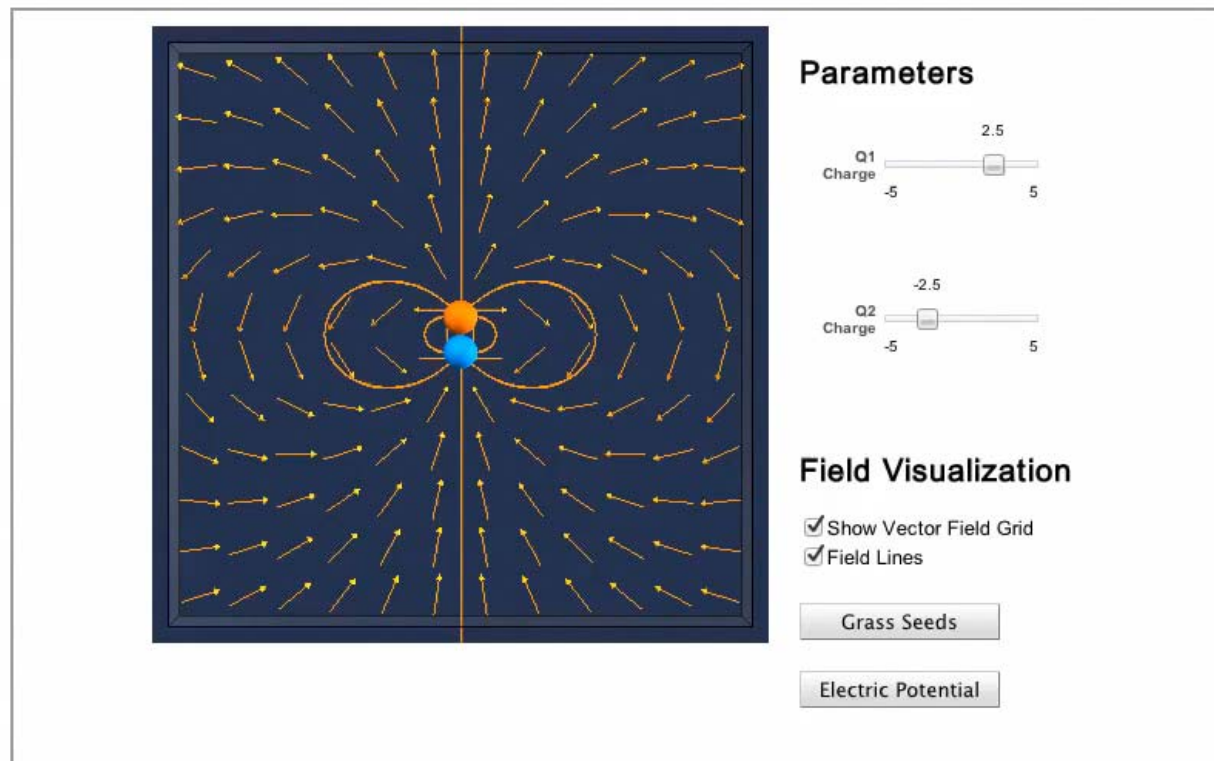
# Do One: Sharpening intuition

## TEALSim Exploration: Point Charges

This simulation illustrates the field pattern created by two point charges with opposite signs of charge. In this simulation, the position and charge of each particle can be modified in real time, and the field configuration will update itself accordingly.

All three field visualization techniques can be applied to show the overall electric field of the two-charge configuration: vector field, field lines, and "grass seeds".

(Please be patient - the simulation may take ~20 seconds to load)



**Parameters**

Q1 Charge: 2.5 (range: -5 to 5)

Q2 Charge: -2.5 (range: -5 to 5)

**Field Visualization**

- Show Vector Field Grid
- Field Lines

Grass Seeds

Electric Potential


More about this simulation: [show](#)



# Do One: Muscle memory

strings.

I was trying to draw my favorite molecule, caffeine. Unfortunately, I'm not a very good biochemist. Can you correct my molecule?



Unit Identifier:  
1f0144c8b1c34d069

New Section Name

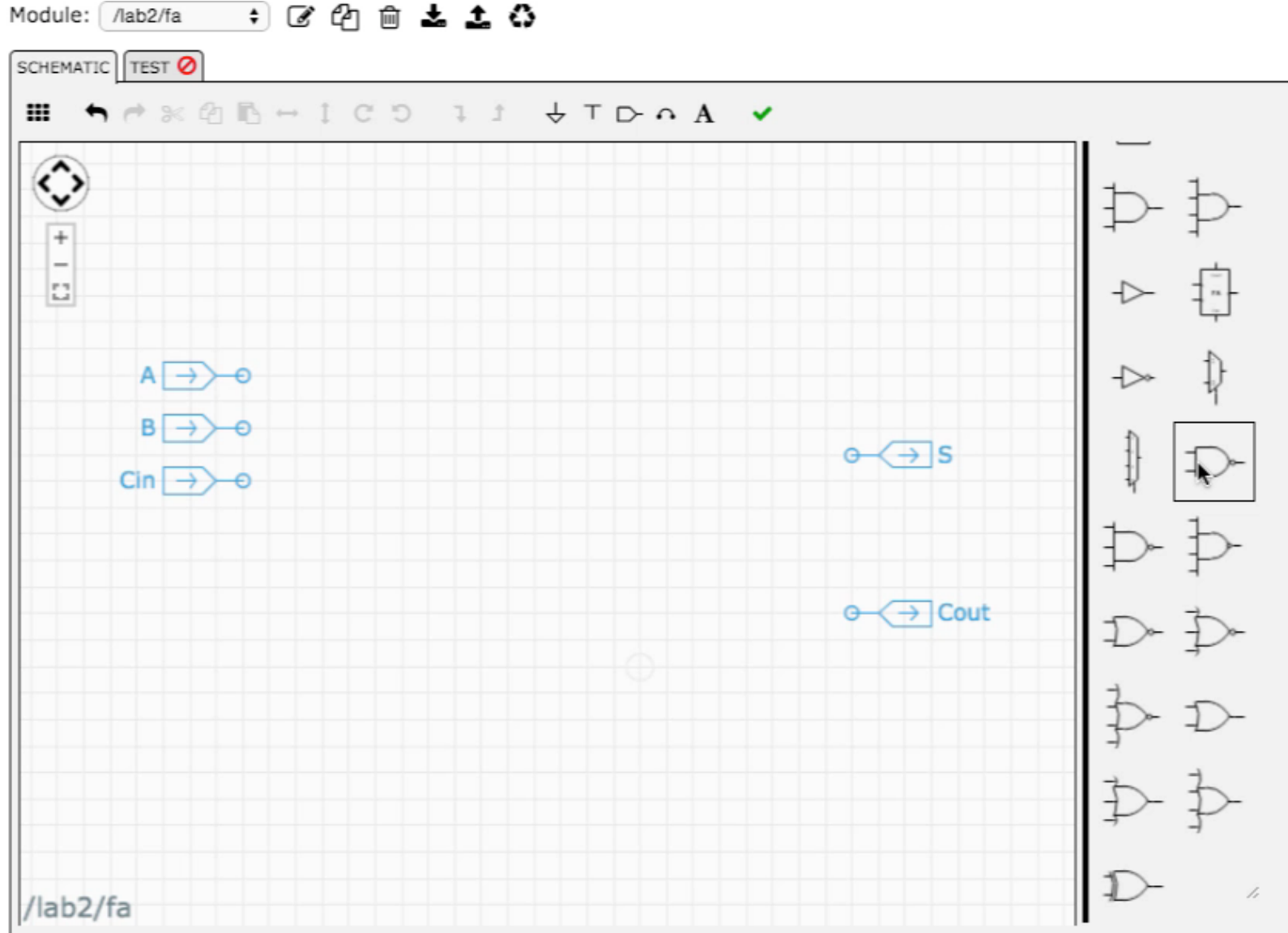
New Subject

New Unit

+ New Unit



# Do One: Starting with a clean slate



/lab2/nand2: drag onto diagram to insert, double click to edit

[Jade 2.2.37 \(2015 © MIT EECS\)](#)

## Challenge: Providing “over-the-shoulder” help



# Teach One: A culture of teaching

## Teaching teaches the teacher

The screenshot shows the Piazza Q&A interface. The top navigation bar includes 'piazza', '6.004', 'Q & A', 'Resources', 'Statistics', and 'Manage Class'. The user 'Chris Terman' is logged in. The left sidebar shows a list of questions, with 'Spring 2014 Q2 4E' selected. The main content area displays the question: 'Spring 2014 Q2 4E' with the text 'I thought that E1 would work, because you just add XL right after the A input and surround it with two registers, and make tCLK = 3ns. How is E4 better and how does it work? I can't visualize what the answer is describing.' Below the question is an 'edit' button, a 'good question' badge with '0' votes, and a timestamp 'Updated 3 days ago by Anonymous'. The answer section is titled 'the students' answer, where students collectively construct a single answer. The answer text reads: 'Remember that THROUGHPUT is  $1 / t\_CLK$ . In part D,  $t\_CLK$  is 1 ns, so throughput is  $1/ns$ . In part E, we're told that we need to keep the same throughput. Therefore, increasing  $t\_CLK$  to 3 ns is unacceptable, since then the throughput would be  $1/3 * 1/ns$ . E4 says to interleave 3 of the XL modules, similar to how we interleaved two modules in lecture (see slides 17 to 19 of lecture 7). This creates a module which acts like an XL module but uses 3 stages. It allows us to keep using  $t\_CLK = 1$  ns, so we can maintain the same throughput as before.' Below the answer is an 'edit' button, a 'good answer' badge with '1' vote, and a timestamp 'Updated 3 days ago by Anonymous'. At the bottom, a summary bar shows 'Average Response Time: 13 min', 'Special Mentions: John Parsons answered Where can we see... in 4 min...', and 'Online Now | This Week: 2 | 212'.

## Challenge: the “M” in MOOC



# Teach One: The wisdom of crowds

Check-off file	Node(s)	Time (ns)	Hint	Upvote Here	Give A Hint
lab6basicblock.	ma[31:0]	399	Look at the bus and pay attention to the...		<a href="#">give a new hint for this error</a>
lab6basicblock.	ma[31:0]	399	it could also be that your bus...	1 <a href="#">upvote</a>	<a href="#">give a new hint for this error</a>
	ma[31:0]	399	Check that your ALU is functioning correctly - it's possible to pass Lab 3's checkoff without actually having a fully functional ALU	0 <a href="#">upvote</a>	<a href="#">give a new hint for this error</a>
lab6basicblock.	mwd[31:0]	1499	It's most likely a problem with your REGFILE. Make sure you're handling R31 correctly both for radata and rdata.	3 <a href="#">upvote</a>	<a href="#">give a new hint for this error</a>
lab6basicblock.	mwd[31:0]	1499	make sure d0 in your mux4 for wdsel is connected to gnd, not ia[31:0].	<a href="#">upvote</a>	<a href="#">give a new hint for this error</a>
	mwd[31:0]	1499	Remember that wmd should be connected to one of the output of the regfile, and not the wd of the regfile itself	<a href="#">upvote</a>	<a href="#">give a new hint for this error</a>
	mwd[31:0]	499	mwd is the memory write address. It is not the same thing as the memory you...		<a href="#">give a new hint for this error</a>

Students add hints for errors they encounter and resolve.

Students upvote hints they find helpful.

Hints are indexed by failed test case.

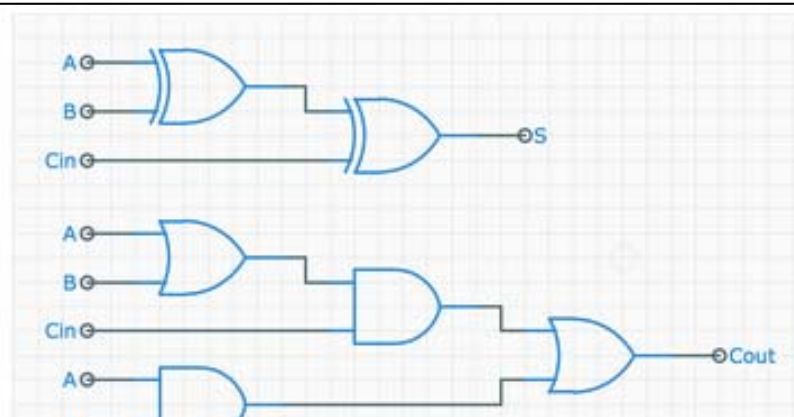


# Teach One: Reflect and advise

## Comparison #1:

If we used the design shown at the right for the FA module, a 3-bit adder would require **132** mosfets, larger than your design by 18 mosfets.

Imagine you're an LA in a future semester of 6.004 and a student submits a solution like the shown on the right. What advice would you give them on how to make their solution as good as yours?

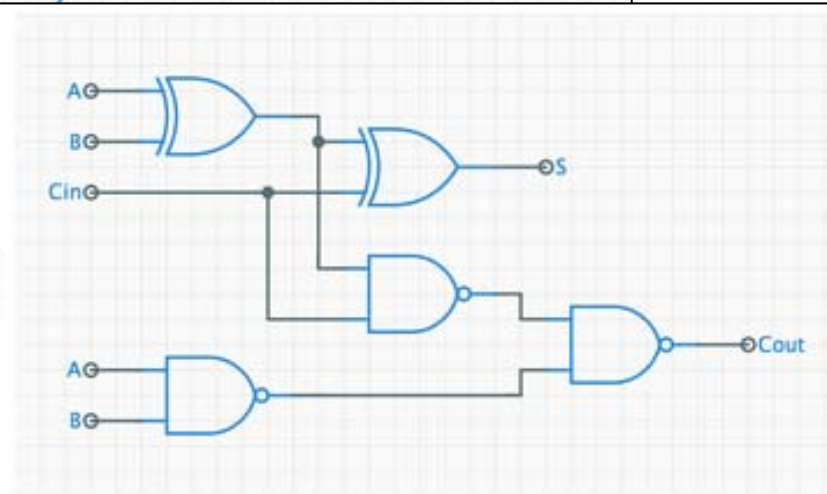


## Comparison #2:

... ente

If we used the design shown at the right for the FA module, a 3-bit adder would require only **96** mosfets, smaller than your design by 18 mosfets.

Imagine you're an LA in a future semester of 6.004 and a student submits a solution like yours. What advice would you give them on how to make their solution as good as the one in the figure to the right?



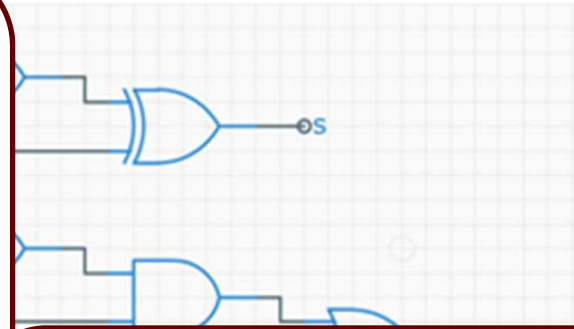
... enter your advice here



# Teach One: Reflect and advise

Co  
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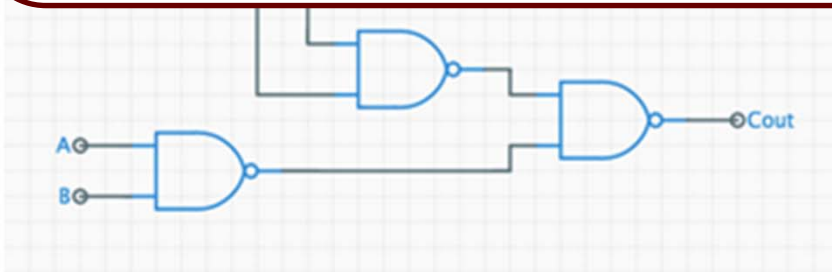
"Mutate the boolean function for  $C_{out}$  such that all OR and AND operations are being NOT'ed. This allows you to design a circuit using only naturally inverting CMOS gates."



"Do not try to be too clever with  $C_{out}$ ---design your schematic as the expression is written. This way you will achieve the [standard] schematic."

... enter **Comparison #2:**

"I would ask: is there a way for you to use some intermediate node in one circuit to bypass a CMOS gate in the other, leading to a reduction of used mosfets?"

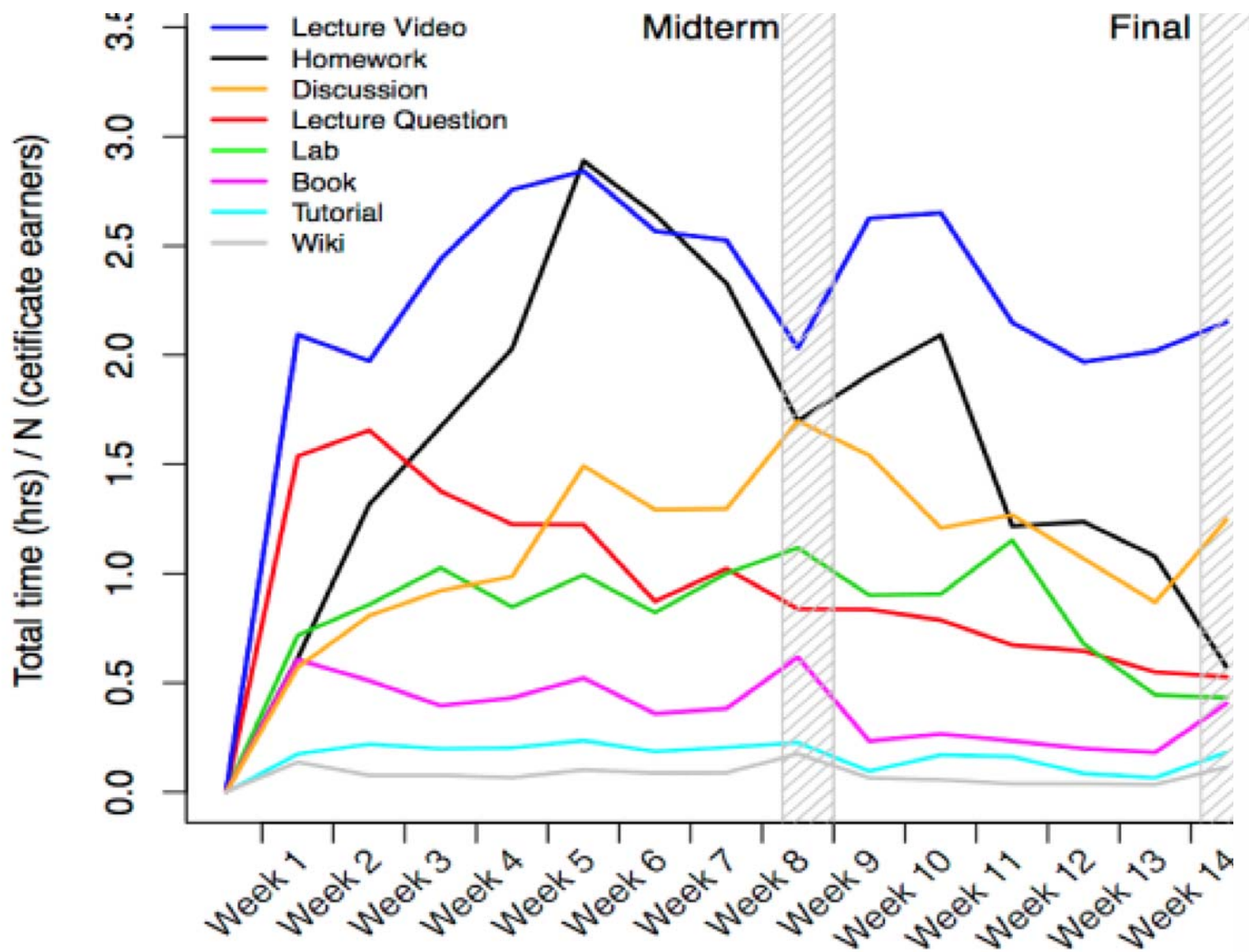


enter your advice here

While the reflection exercise itself is valuable, these hints could also be passed on to other students.



# How students invest their time

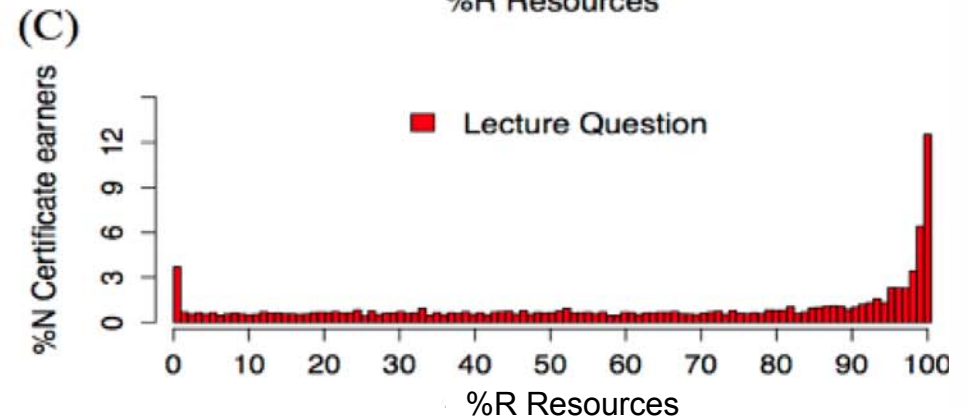
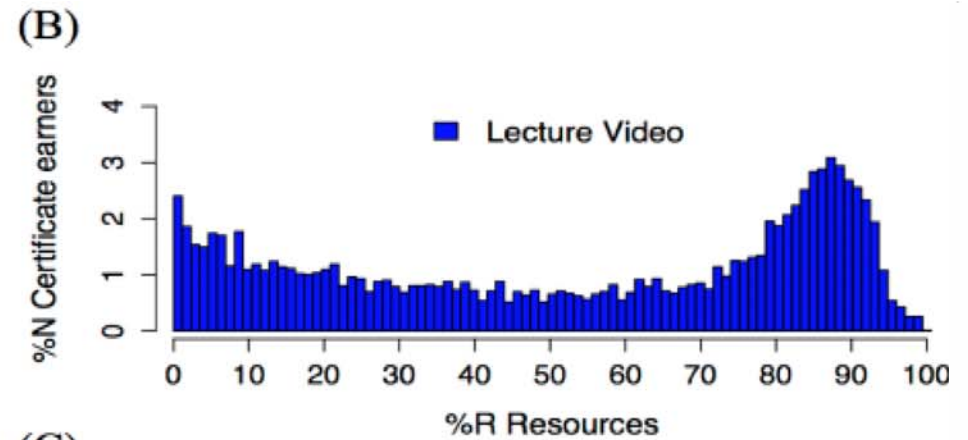
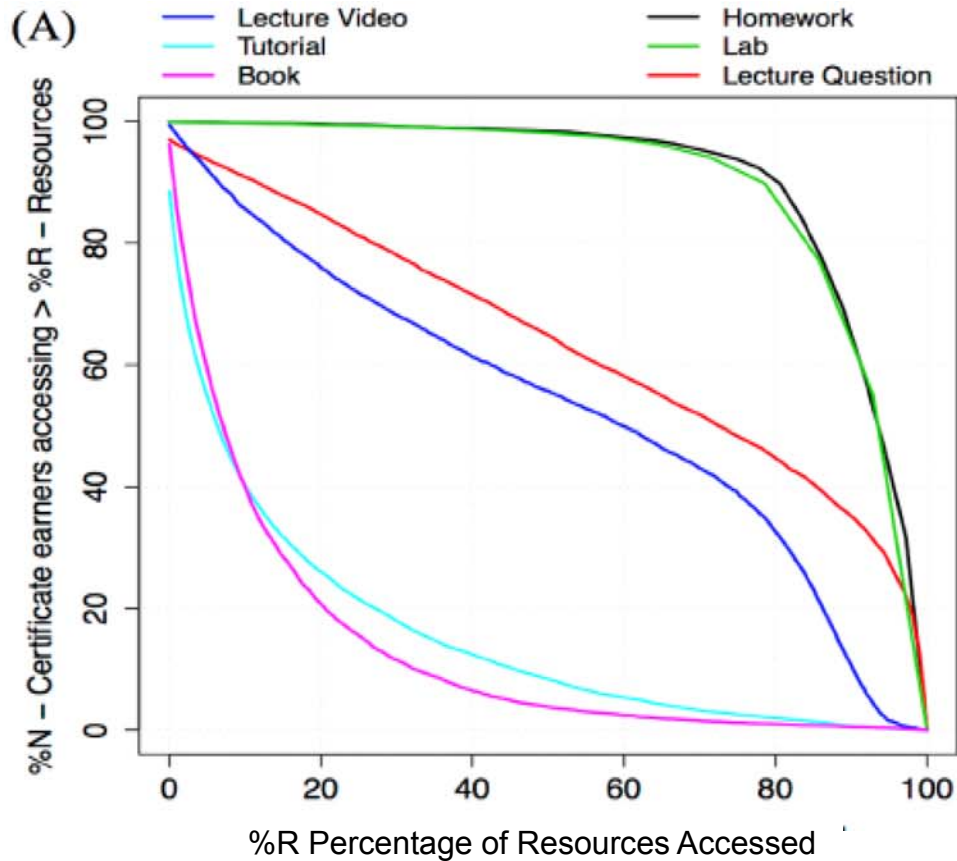


6.002x w/ Dave Pritchard (<http://RELATE.mit.edu>)





# The educational buffet

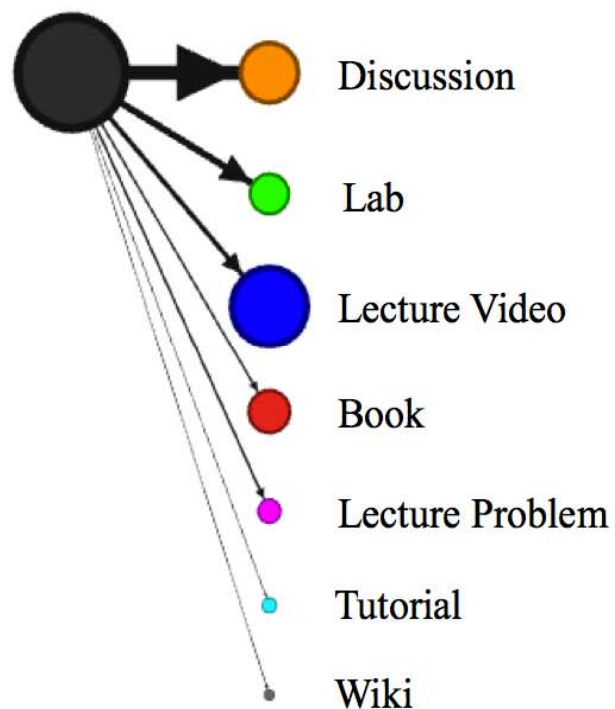


6.002x w/ Dave Pritchard (<http://RELATE.mit.edu>)

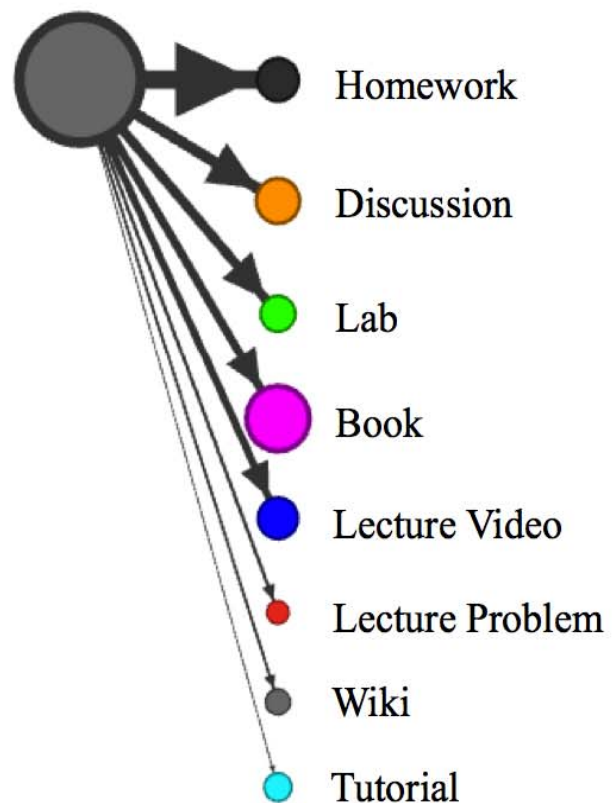


# Assessment driven?

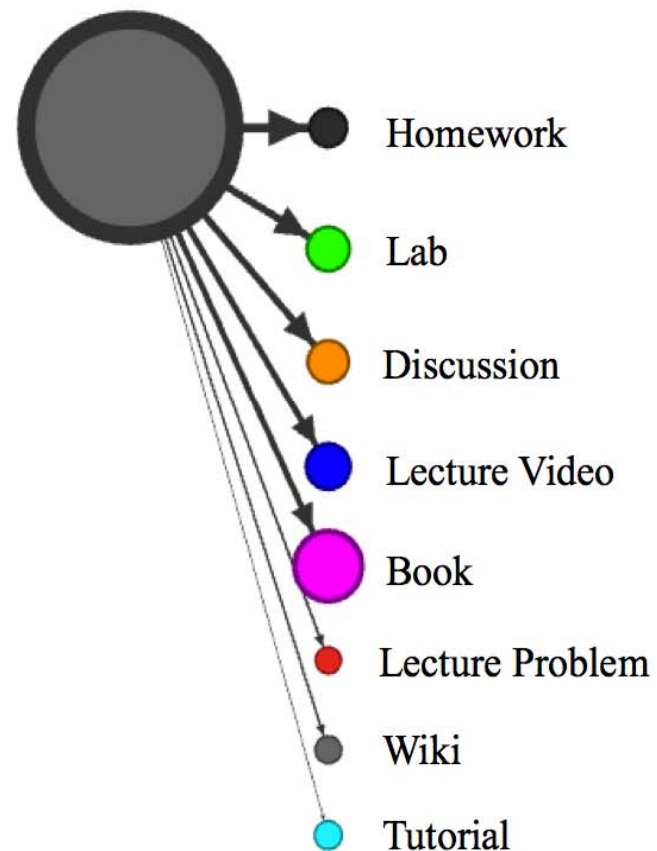
(A) Homework



(B) Midterm Exam



(C) Final Exam

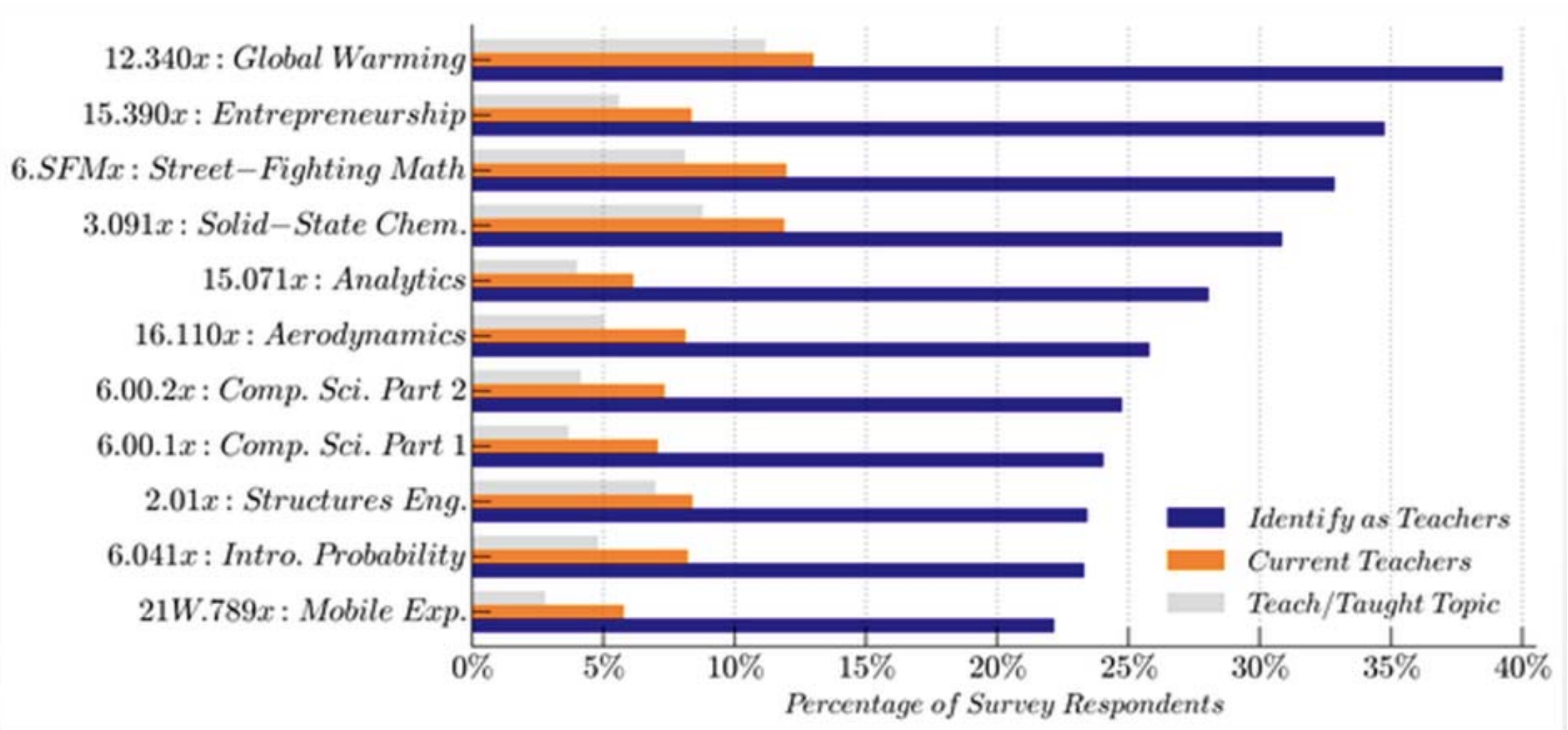


6.002x w/ Dave Pritchard (<http://RELATE.mit.edu>)



# Teaching the teachers

Results about learner background from entry/exit surveys for MITx courses:



<http://www.educause.edu/ero/article/enrollment-mitx-moocs-are-we-educating-educators>

