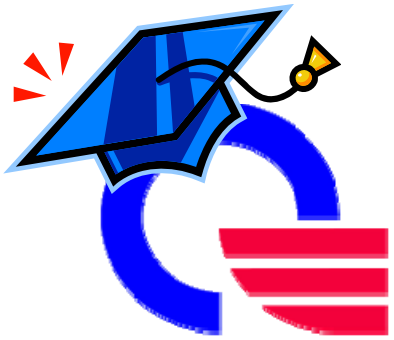
MIT COMPUTER SCIENCE AND ARTIFICIAL INTELLIGENCE LABORATORY



See One, Do One, Teach One

Chris Terman

Senior Lecturer, MIT Dept. of EECS

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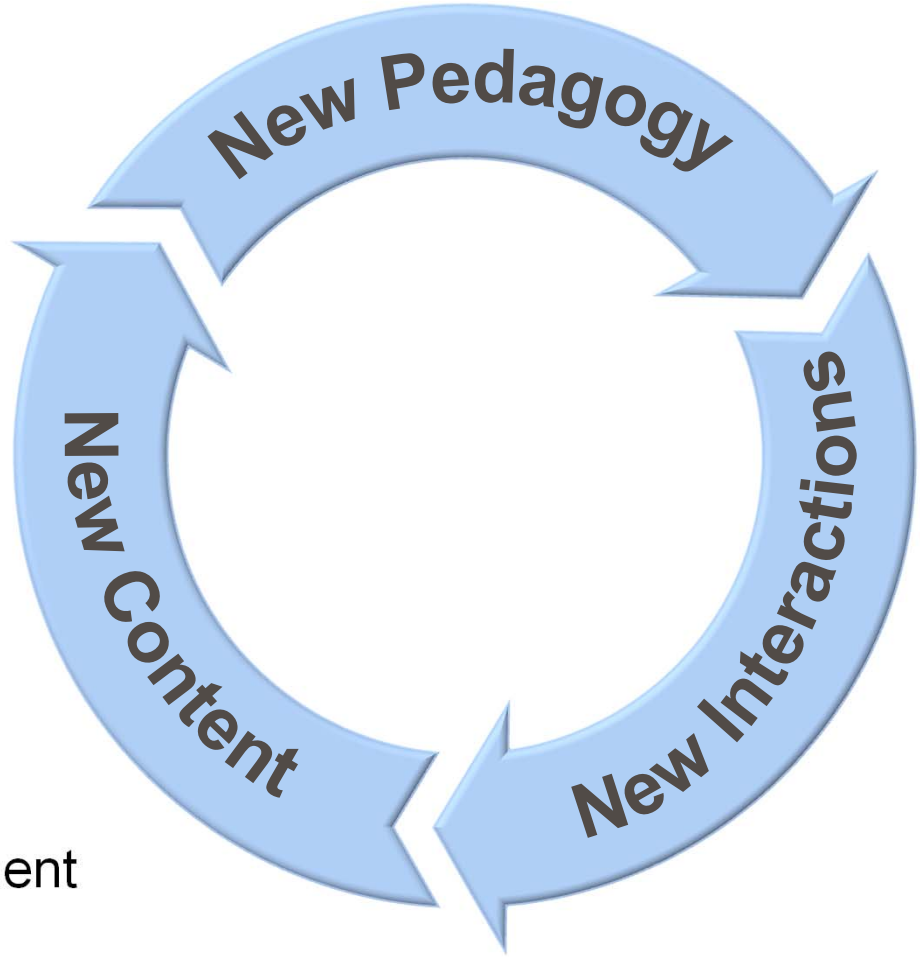
Research in Educational Technology @ CSAIL

- Self-paced mastery learning
- Hands-on learning
- MOOC as education laboratories
- Measure results → target improvements



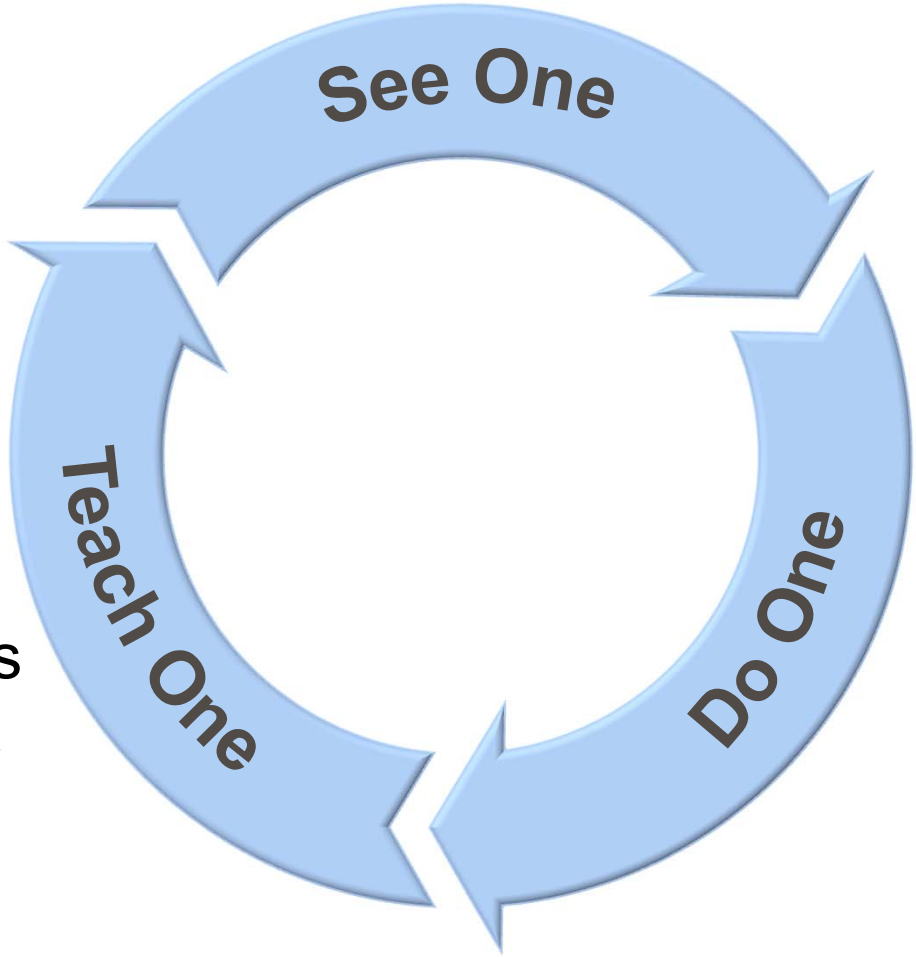
- Curricular API
- Authoring tools
  - Visualizations
  - Interactions
- Automate assessment

- Forum summaries
- Search/navigation
- Learning networks
- Learner sourcing

Achieving mastery

Novice

- Learn concepts
- Observe skills
- Analyze
- Understand ***what***



Master

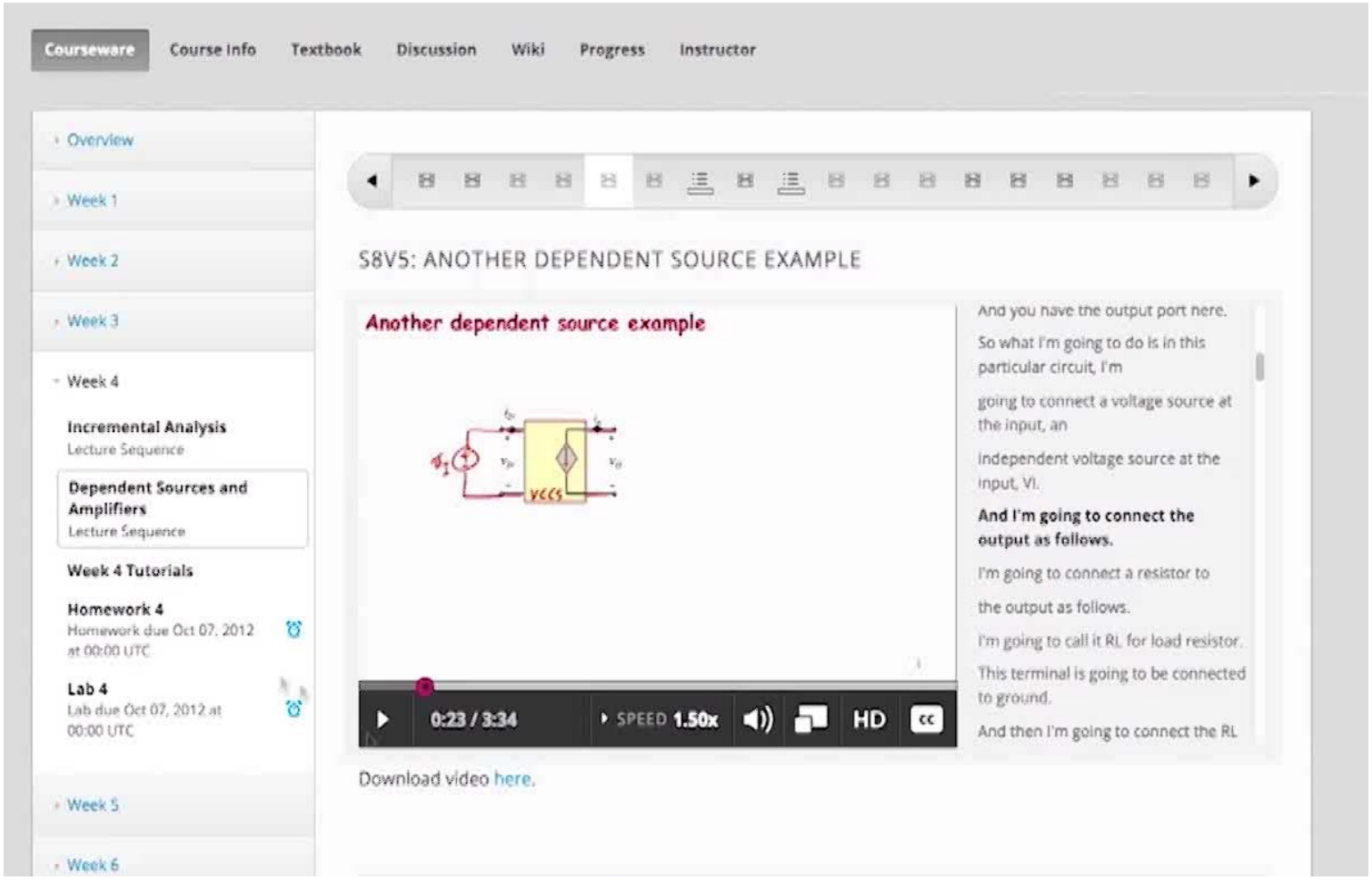
- Teach concepts
- Demonstrate skills
- Organize/connect
- Explain ***why***

Apprentice

- Apply concepts
- Practice skills
- Synthesize
- Learn ***how***

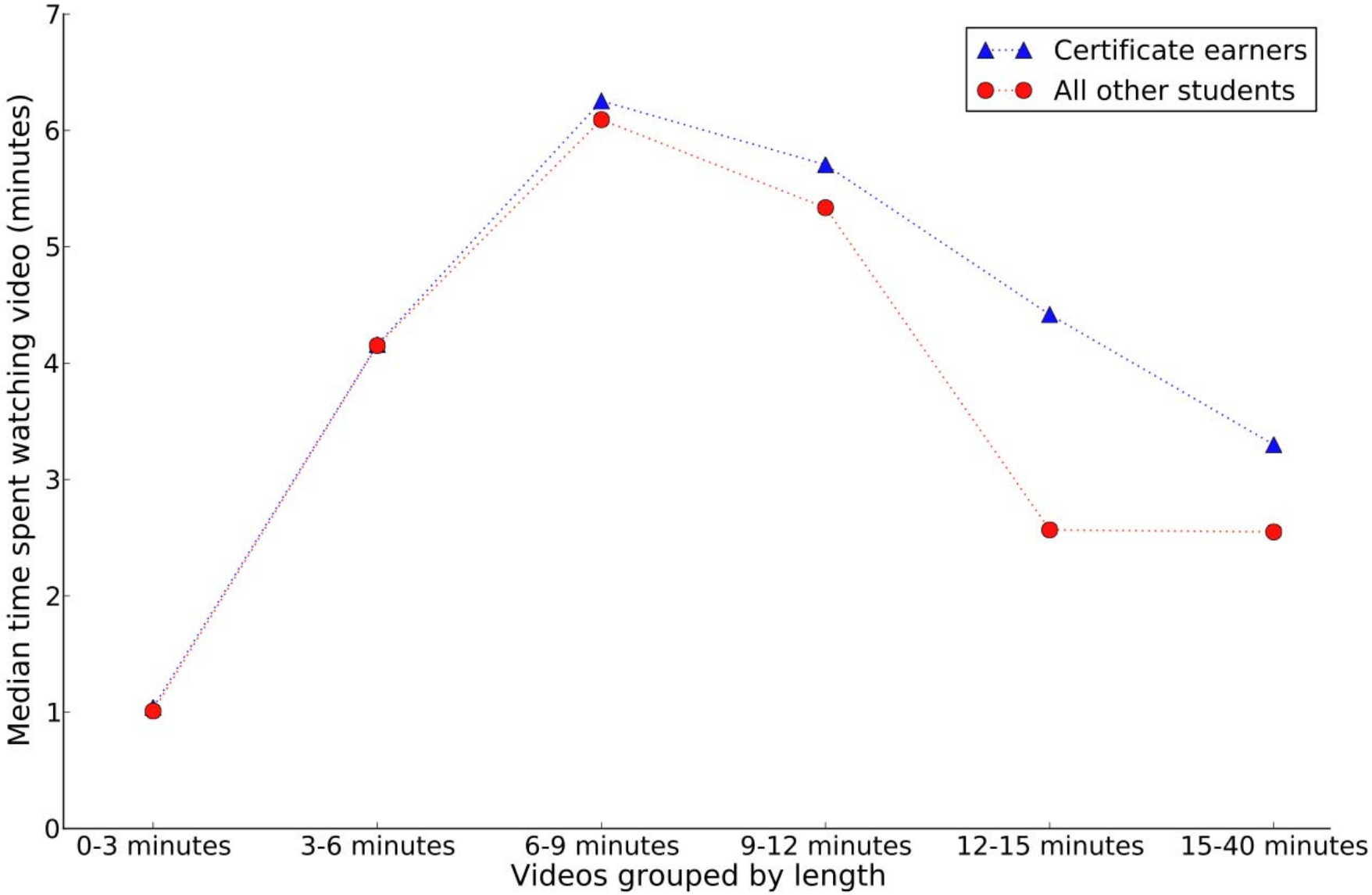
See One: Effective learning sequences

Recipe: Short video → interaction → repeat



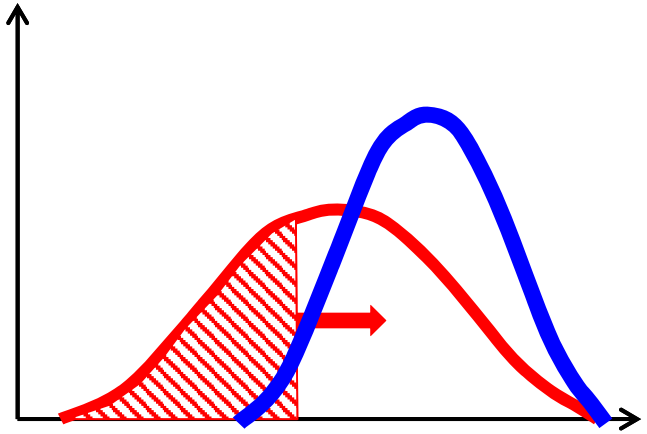
Challenge: it's not a captive audience!

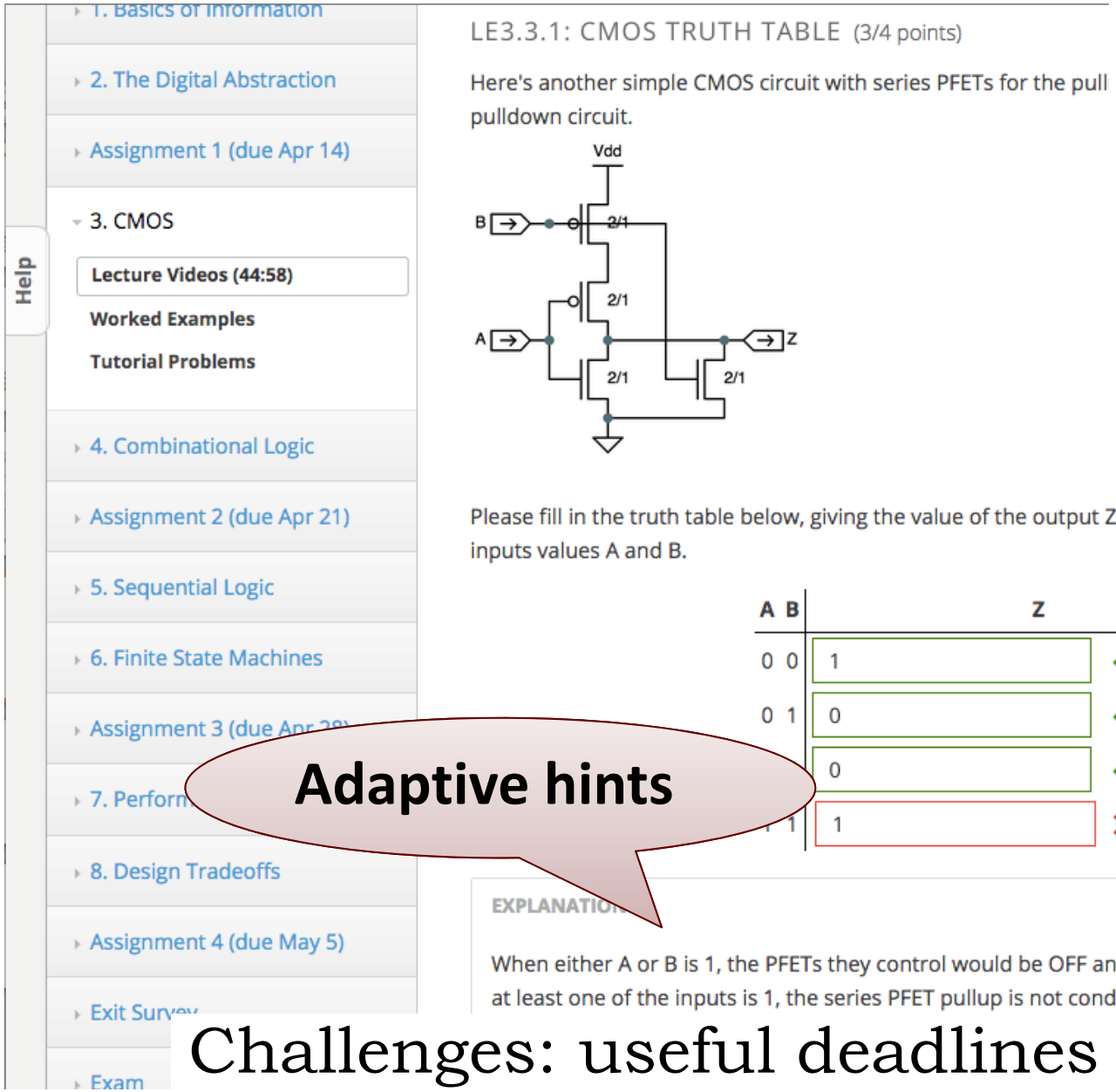
See One: Attention span data



Philip Guo (http://www.pgbovine.net/)

See One: Mastery learning





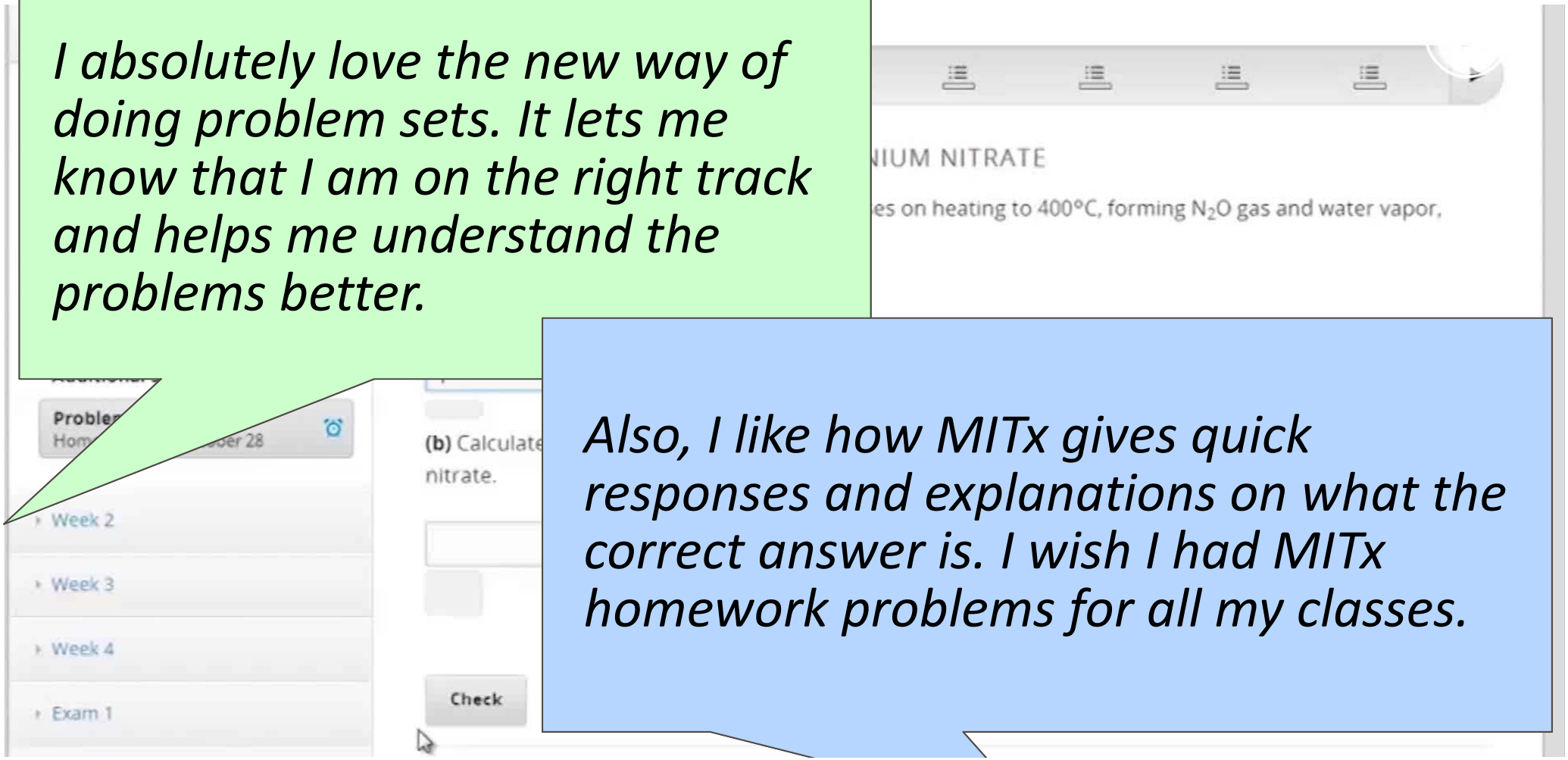
Adaptive hints

Challenges: useful deadlines & cohorts

See One: Immediate feedback

Go to go? Or more work to be done?

I absolutely love the new way of doing problem sets. It lets me know that I am on the right track and helps me understand the problems better.



Also, I like how MITx gives quick responses and explanations on what the correct answer is. I wish I had MITx homework problems for all my classes.

Challenge: avoiding "guess and check"

Do One: Hands On → Brain On!

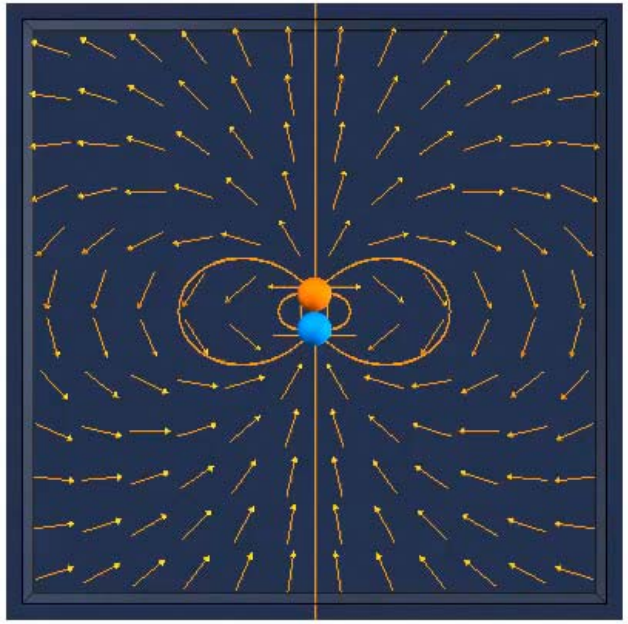
> Learning and retention is related to the depth of mental processing.
> - *Craik and Lockhart 1972*

Do One: Sharpening intuition

TEALSim Exploration: Point Charges

This simulation illustrates the field pattern created by two point charges with opposite signs of charge. In this simulation, the position and charge of each particle can be modified in real time, and the field configuration will update itself accordingly.
All three field visualization techniques can be applied to show the overall electric field of the two-charge configuration: vector field, field lines, and "grass seeds".

(Please be patient - the simulation may take ~20 seconds to load)



Parameters

Q1 Charge: 2.5 (-5 to 5)

Q2 Charge: -2.5 (-5 to 5)

Field Visualization

- ☑ Show Vector Field Grid
- ☑ Field Lines

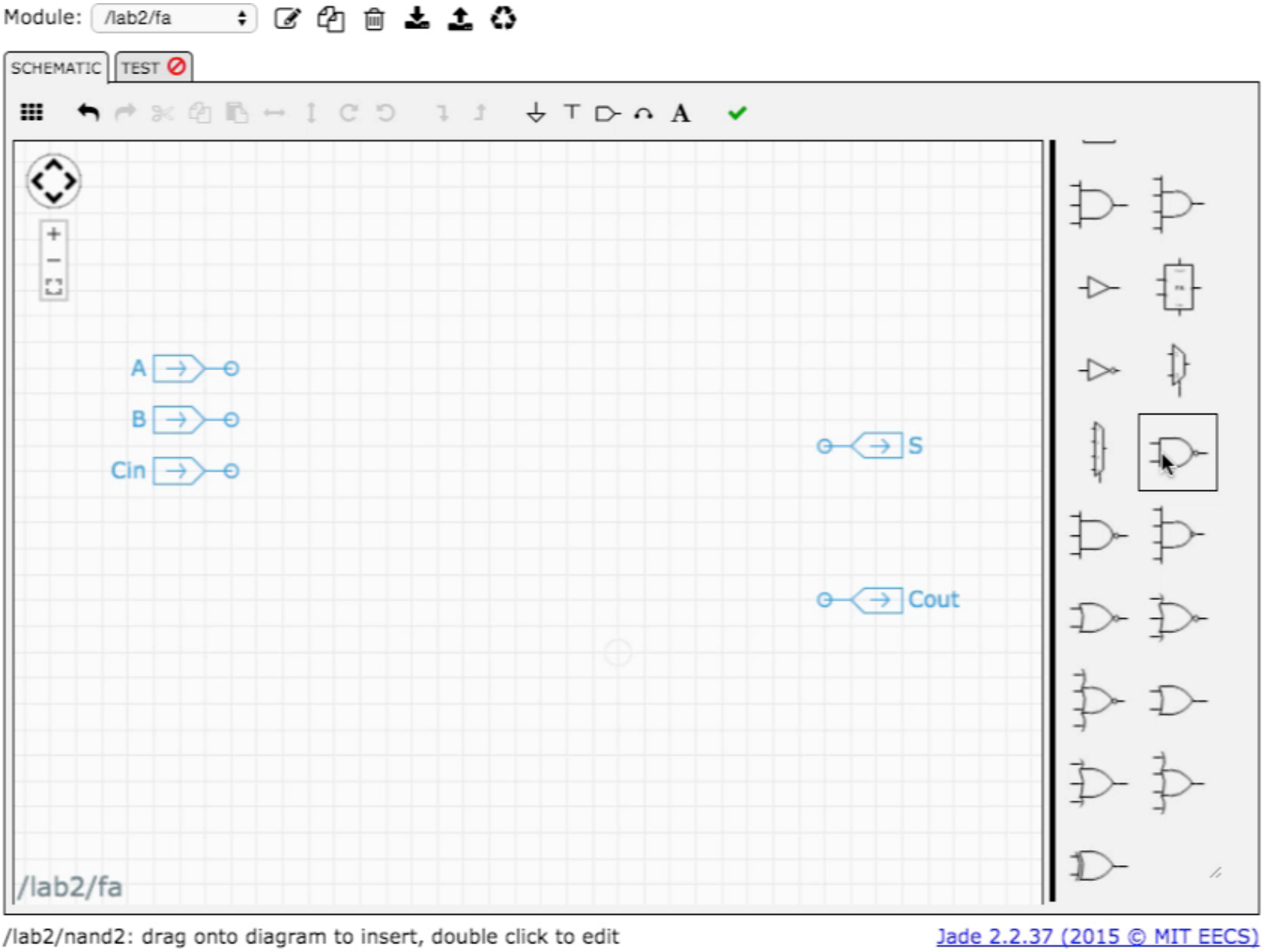
Grass Seeds

Electric Potential

More about this simulation: show

Do One: Muscle memory

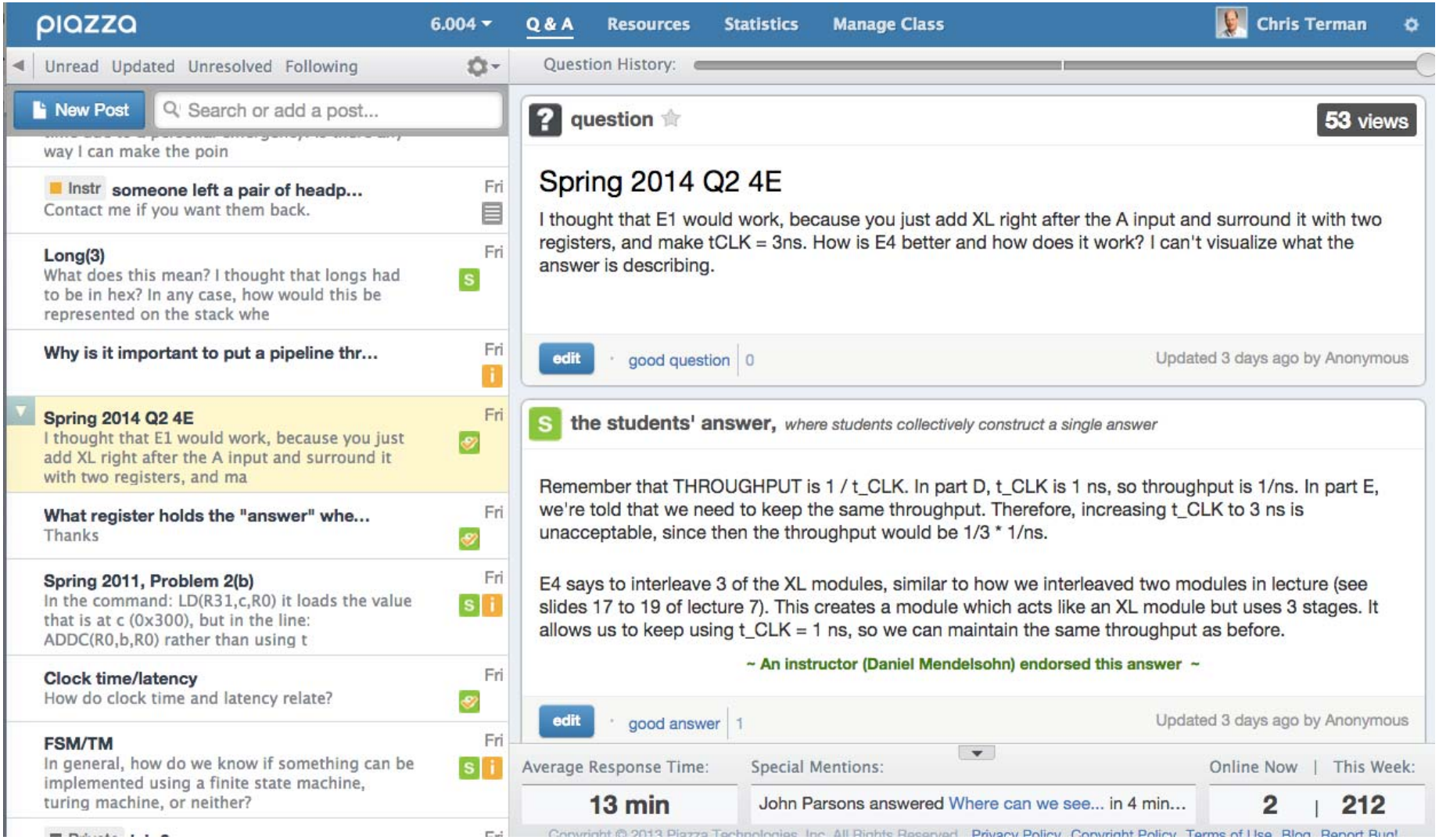
Do One: Starting with a clean slate



Challenge: Providing "over-the-shoulder" help

Teach One: A culture of teaching

Teaching teaches the teacher



Challenge: the “M” in MOOC

Teach One: The wisdom of crowds

Check-off file	Node(s)	Time (ns)	Hint	Upvote Here	Give A Hint
			If you wer… wo…		…ur own …n
lab6basicblock.	ma[31:0]	399	Look … pay attention to the …		…w hint for this error
lab6basicblock.	ma[31:0]	399	it could also be that your bs… …ng	1 upvote	give a new hint for this error
	ma[31:0]	399	Check that your ALU is functioning correctly - it's possible to pass Lab 3's checkoff without actually having a fully functional ALU	0 upvote	give a new hint for this error
lab6basicblock.	mwd[31:0]	1499	It's most likely a problem with your REGFILE. Make sure you're handling R31 correctly both for radata and rbdata.	3 upvote	give a new hint for this error
lab6basicblock.	mwd[31:0]	1499	make sure d0 in your mux4 for wdsel is connected to gnd, not ia[31:0].	…upvote	give a new hint for this error
	mwd[31:0]	1499	Remember that wmd should be connected to one of the output of the regfile, and not the wd of the regfile itself	…pvote	give a new hint for this error
	mwd[31:…	…499	mwd is the memory write address. It is … same thing as the memory yo… registers. …t about BSEL!		…new hint …or

Students add hints for errors they encounter and resolve.

Students upvote hints they find helpful.

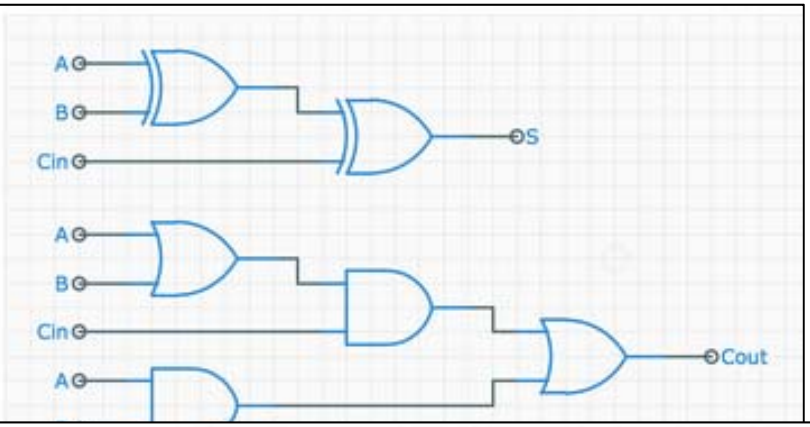
Hints are indexed by failed test case.

Teach One: Reflect and advise

Comparison #1:

If we used the design shown at the right for the FA module, a 3-bit adder would require **132** mosfets, larger than your design by 18 mosfets.

Imagine you're an LA in a future semester of 6.004 and a student submits a solution like the shown on the right. What advice would you give them on how to make their solution as good as yours?

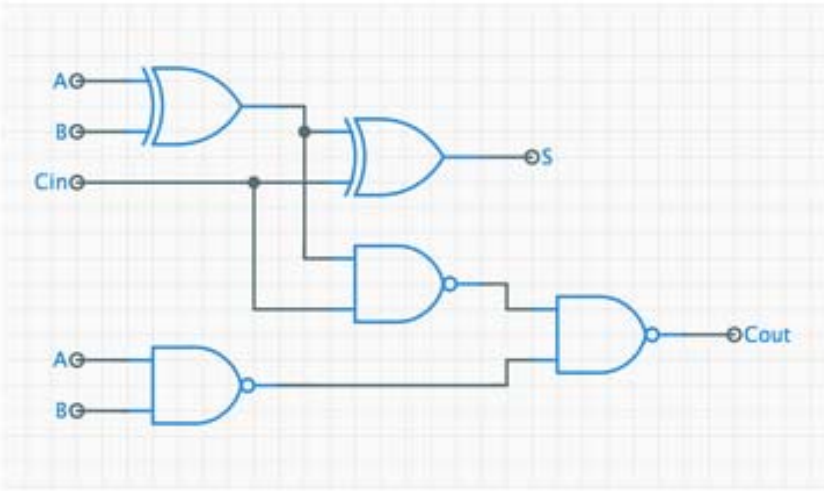


... ente

Comparison #2:

If we used the design shown at the right for the FA module, a 3-bit adder would require only **96** mosfets, smaller than your design by 18 mosfets.

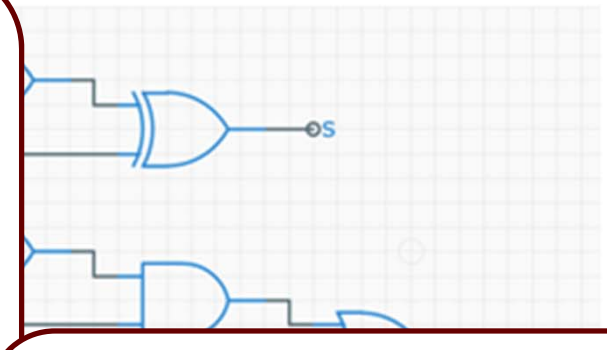
Imagine you're an LA in a future semester of 6.004 and a student submits a solution like yours. What advice would you give them on how to make their solution as good as the one in the figure to the right?



... enter your advice here

Teach One: Reflect and advise

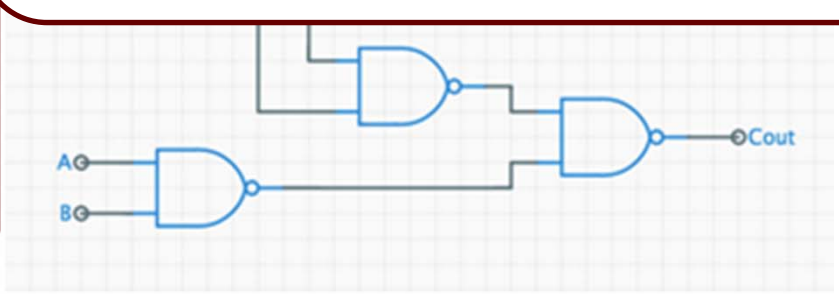
"Mutate the boolean function for C_{out} such that all OR and AND operations are being NOT'ed. This allows you to design a circuit using only naturally inverting CMOS gates."



"Do not try to be too clever with C_{out}---design your schematic as the expression is written. This way you will achieve the [standard] schematic."

... enter **Comparison #2:**

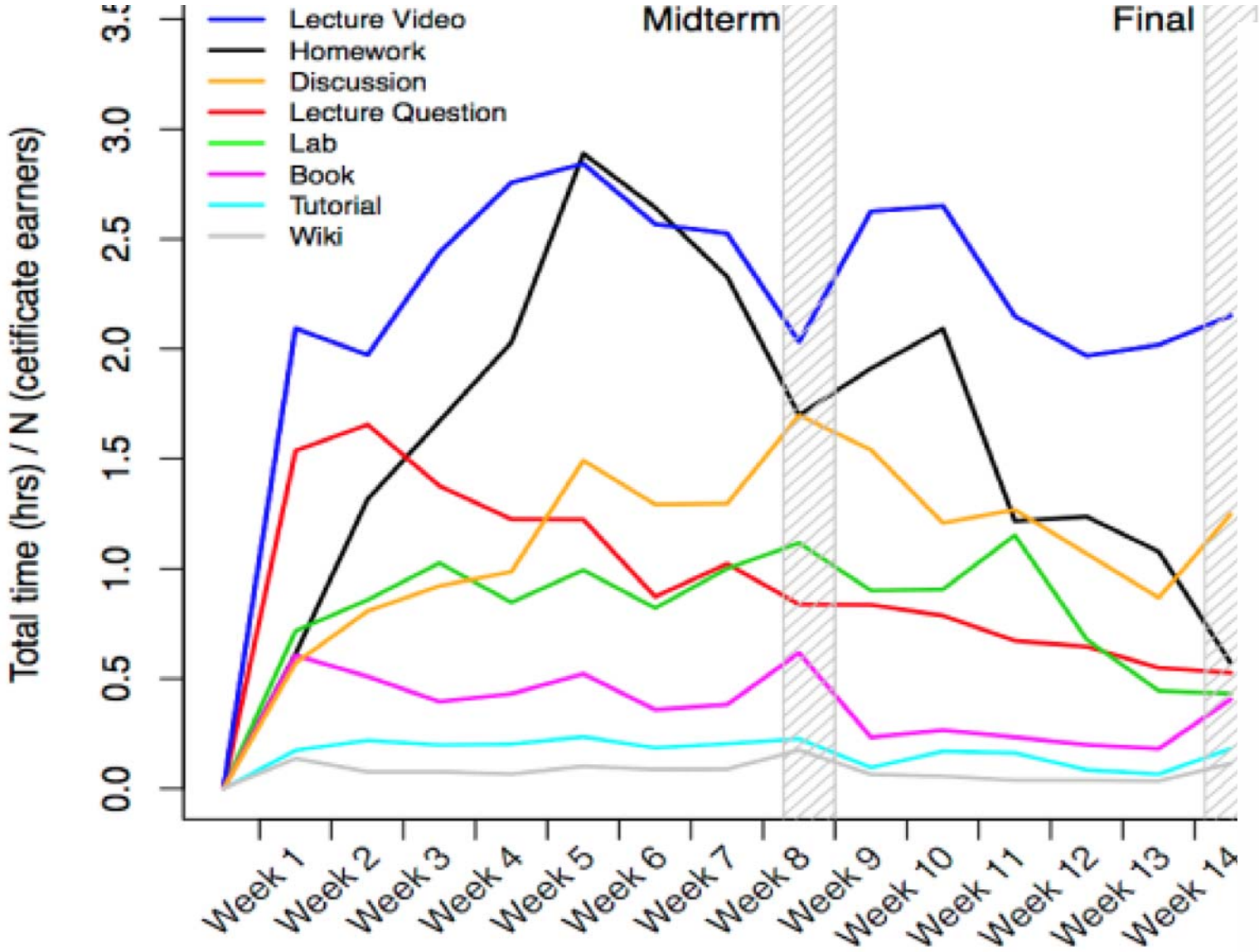
"I would ask: is there a way for you to use some intermediate node in one circuit to bypass a CMOS gate in the other, leading to a reduction of used mosfets?"



enter your advice here

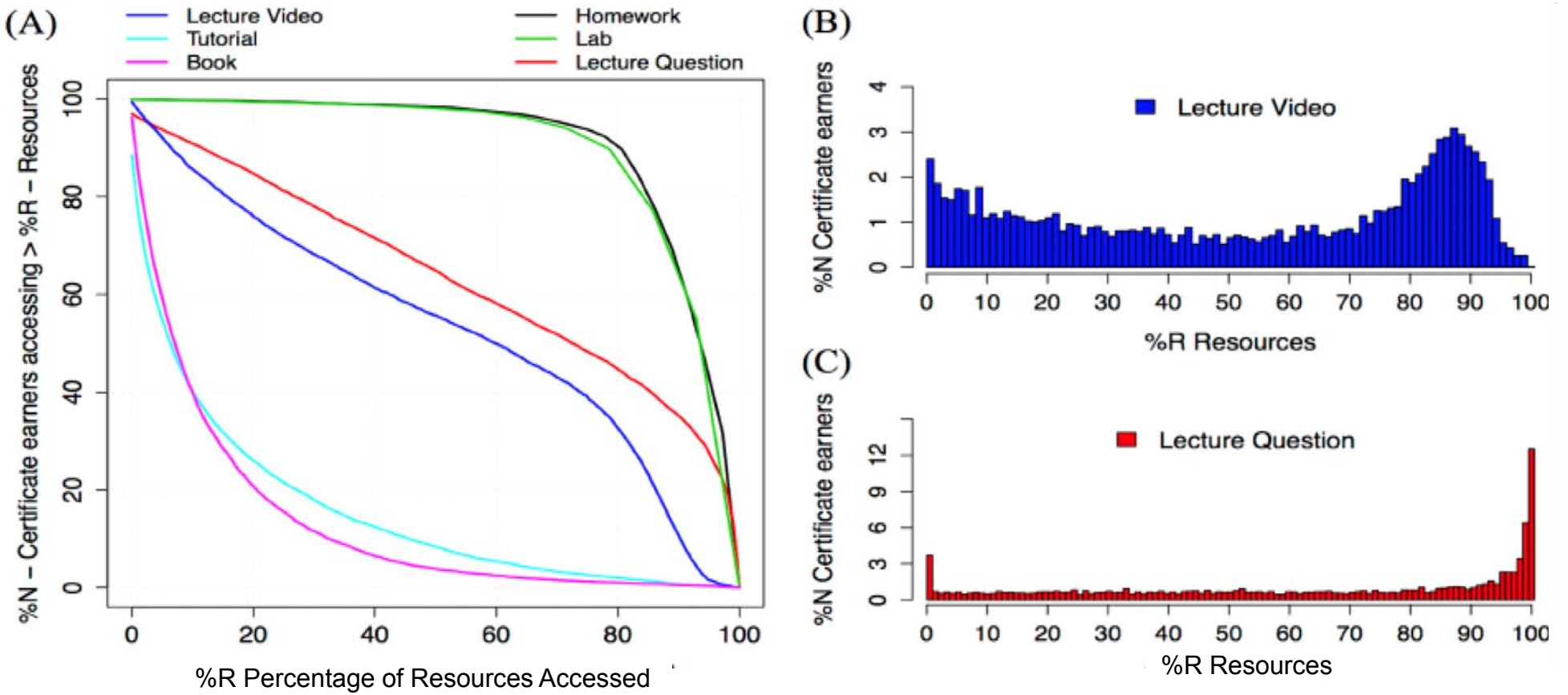
While the reflection exercise itself is valuable, these hints could also be passed on to other students.

How students invest their time



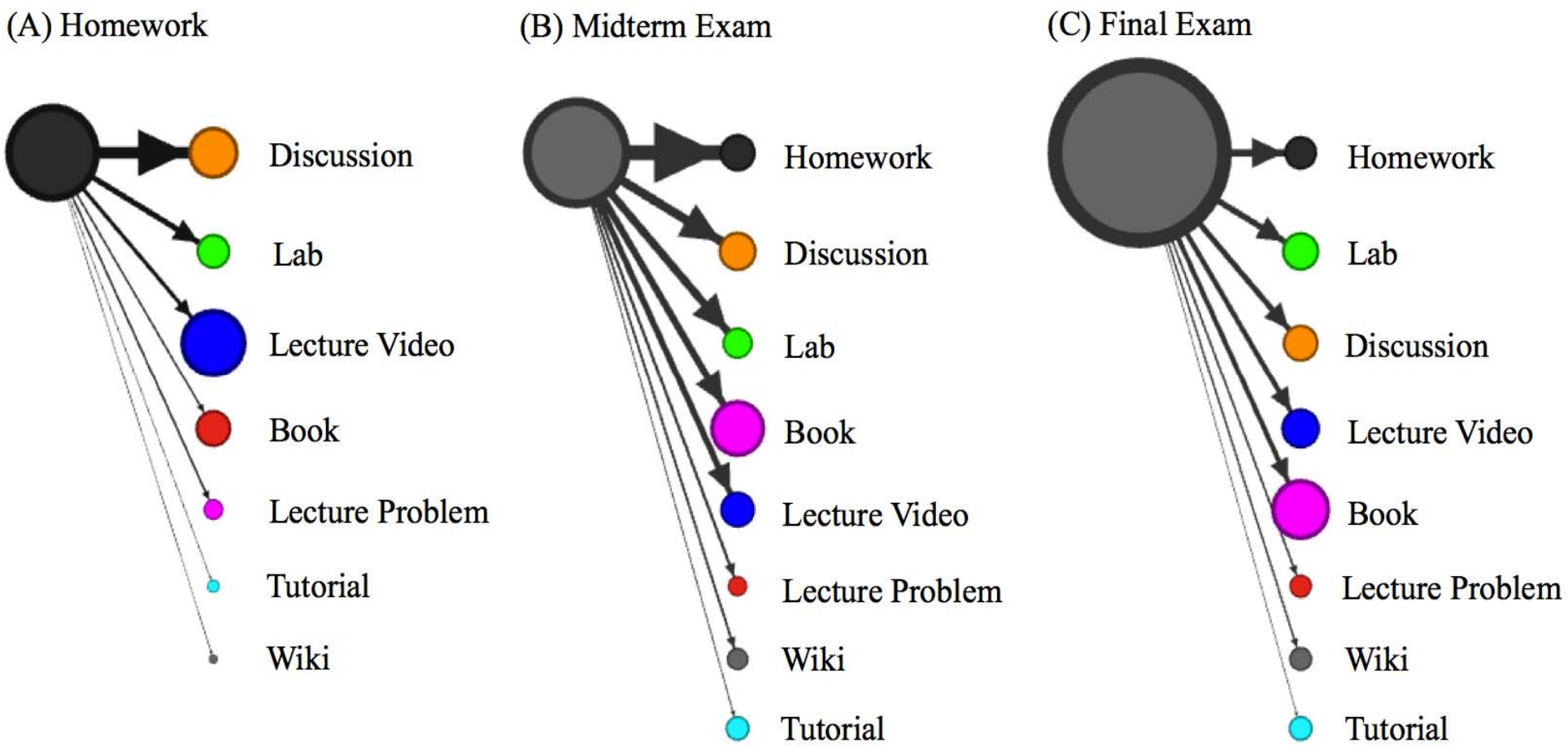
6.002x w/ Dave Pritchard (http://RELATE.mit.edu)

The educational buffet



6.002x w/ Dave Pritchard (http://RELATE.mit.edu)

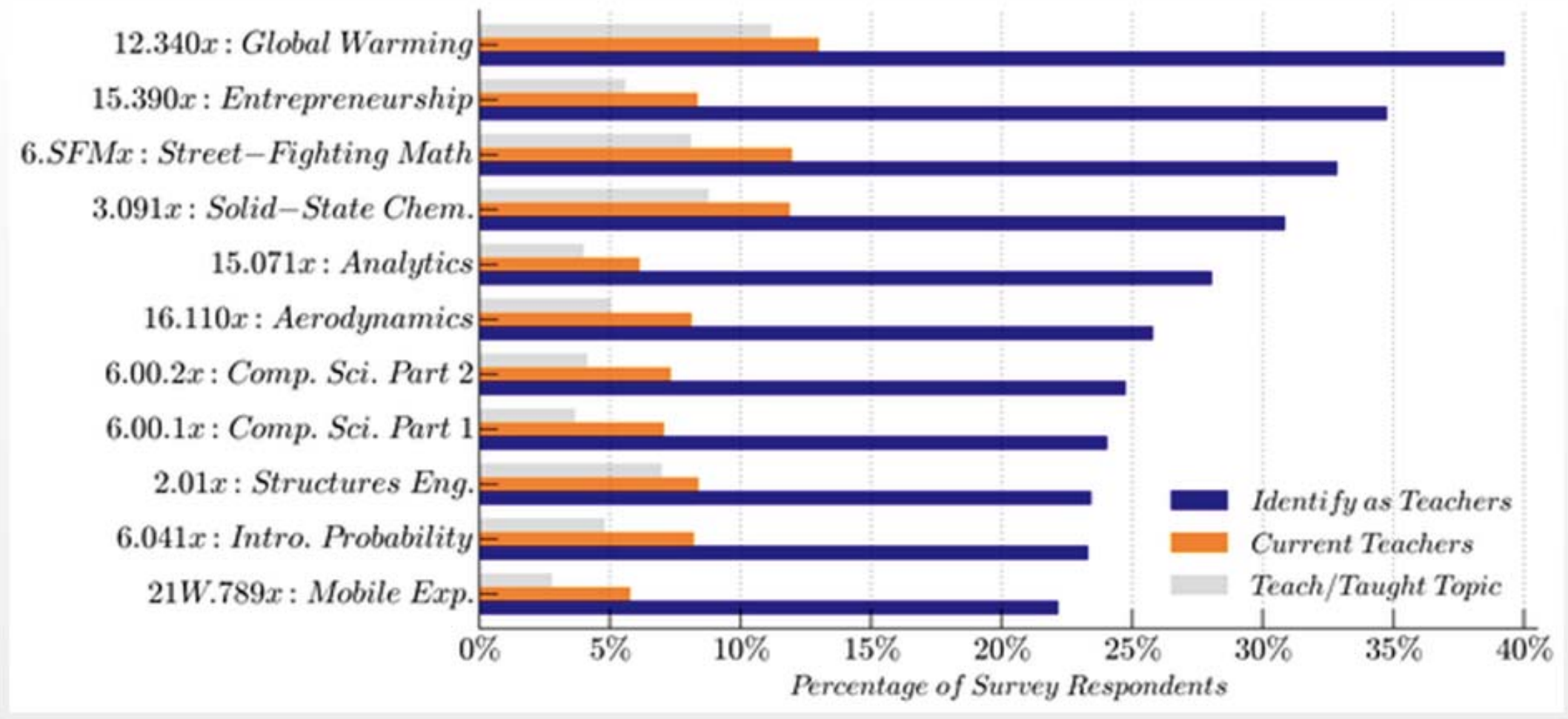
Assessment driven?



6.002x w/ Dave Pritchard (http://RELATE.mit.edu)

Teaching the teachers

Results about leaner background from entry/exit surveys for MITx courses:



http://www.educause.edu/ero/article/enrollment-mitx-moocs-are-we-educating-educators